AF/2700 $ #28

Patent 3-19-03 Qw

Attorney's Docket No. 028433-007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Toyohiko YOSHIDA et al.	Group Art Unit: 2183
Application No.: 09/146,259	Examiner: W. Treat
Filed: September 3, 1998	Confirmation No.: 2183
For: DATA PROCESSING DEVICE	

REQUEST FOR ORAL HEARING

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants, through the undersigned, hereby request that an oral hearing be scheduled before the U.S. Patent and Trademark Office Board of Appeals in connection with the subject application.

A check in the amount of [ ] $140.00 (2403) [X] $280.00 (1403) is attached hereto to cover the requisite Government fee. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
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Registration No. 32,131

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Date: March 14, 2003

(05/02)

Patent
Attorney's Docket No. 028433-007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Toyohiko YOSHIDA et al.	)	Confirmation No: 7001
	)	
Application No.: 09/146,259	)	Group Art Unit: 2183
	)	
Filed: September 3, 1998	)	Examiner: W. Treat
	)	
For: DATA PROCESSING DEVICE	)	Appeal No.
	)	
	)	
	)	

REPLY BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: March 14, 2003

Sir:

This Reply Brief is filed in response to the Examiner's Answer dated January 15, 2003 (Paper No. 26). Concurrently filed with this Reply Brief is a Request for Oral Hearing.

In the Examiner's Answer, the Examiner stated that the claims stand or fall together since the Applicants have merely pointed out differences in what the claims cover is not an argument as to why the claims are separately patentable. However, Applicants respectfully note that arguments presented point out the limitations recited in the claims which are not described in the prior art.

Applicants respectfully traverse the Examiner's rejection of claims 1-25 under 35 U.S.C. §112, second paragraph. Applicants do not understand the Examiner's reasoning with regard to page 5 lines 7-11. In particular, a branch is a sub-instruction or operation code found within an instruction word. As described in the specification and in particular with regard to Figures 2a and 2b, an instruction word can contain a single operation code

(i.e., operation, sub-instruction) or may contain two operation codes depending upon whether the instruction word is a dual operation instruction as shown in Fig. 2a or a single operation instruction as shown in Fig. 2b. Thus a branch is an operation code found within an instruction word. The operation code is also called a sub-instruction or operation within the specification. Applicants respectfully point out that branches, compares, etc. are not instruction words but are operation codes found within instruction words. Attached please find the definition of these common terms from a web technical dictionary and in particular the meaning of instruction, and operation code. Additionally, Applicants cannot understand the Examiner's statement on page 7 lines 8-15. The Examiner appears to be reading claim 21 such that the condition instruction is only an operation code that is decoded by one of the decoders 8 and 9. In fact, the condition instruction claimed in claim 21 is an instruction word which is decoded by the instruction decode unit 2. The Examiner's understanding is incorrect and not supported by the description within the specification. Applicants respectfully request the Board reverses the rejection to claims 1-25 under 35 U.S.C. §112 second paragraph.

Applicants again respectfully traverse the Examiner's rejection of claims 1-25 under 35 U.S.C. §112 first paragraph. Applicants cannot understand the Examiner's rejection and specifically traverses the Examiner's statement that the claims mix the capabilities of instructions and sub-instructions without distinguishing as to what provides the capabilities. As claimed in claim 1, an instruction decoder (2) sequentially decodes a plurality of instructions (101, 102) and outputs control signals 11, 12, the instructions execution unit (3, 4) executes operations (106, 107, 108), the instructions decoder decodes a first instruction and outputs a first control signal in a first period (Figure 9, t2), the instruction execution unit, (3, 4) executes the operation designed by the first instruction in a second period (Figure 9, t3), and determines whether or not a predetermined condition is satisfied in a fourth period (Figure 9, t7). The Examiner's attention is brought to Figure 9 and the description found on page 52 line 2 through page 60 line 26 as well as page 63 line 1 through page 70 line 11. Thus, the periods claimed in the claims refer to the clock cycles

shown in Figure 9. Applicants respectfully request the Board reverses the rejection to claims 1-25 under 35 U.S.C. §112, first paragraph.

Applicants again respectfully traverse the Examiner's rejection of claims 1-25 under 35 U.S.C. §102(a) or under 35 U.S.C. §103. The Examiner has pointed to a program that he has submitted as proof that the invention is obvious based upon columns 11, 12 and column 18 lines 45-60 of *Holmann et al.* (U.S. Patent No. 5,815,698). However, this part of *Holmann et al.* merely discusses a processor status word PSW. In particular, *Holmann et al.* at column 18 lines 45-46 merely indicates a delayed instruction processing is to be done. Nothing in *Holmann et al.* shows, teaches or suggests the timing of determining a condition. The Examiner stated that *Holmann et al.* "saves the value of the program counter to be used to compare against the PC in a first register and the hardware faithfully checks to see if the condition is a condition for executing the branch." The Examiner has not explained how a register for holding a condition for executing the branch is the same as a timing for starting a determination of the condition as claimed in claim 14. Please see the specification, page 52, line 19 through page 54, line 21. Additionally, the Examiner's has not addressed claim 1 and merely states that claim 21 fails to define over the rejection of claims 14-16. Nowhere in *Holmann et al.* is it shown, taught or suggested delaying a timing of determining a condition as claimed in claims 1, 14 and 21. Therefore, Applicants respectfully request the Board reverses the Examiner's decision.

The Examiner has again requested that a drawing be submitted to facilitate the understanding of the invention. However, Figure 1 clearly shows registers 31-32 holding the various signals as discussed on page 54 lines 1-21. It is respectfully submitted that Figure 1 already discloses the registers claimed in claims 14, 18 and 20. Applicants note that nowhere is there a requirement that in the absence of the specification that the drawing themselves enable understanding of the claims as suggested by the Examiner. Applicants respectfully request the Board reverses the Examiner's objection to the drawings.

Applicants respectfully traverse the objection to the drawings as lacking suitable legends. The Examiner has not stated precisely what legends he would like to see to designate the 46 registers shown within the drawings. Presently, they are only designated

by number and labeling all registers with the title "register" or R1- etc. would not seem to convey any additional meaning and in fact may make the drawing undecipherable due to too many legends. Applicants respectfully request the Board reverses the Examiner's objection to the drawings or at least explain what labeling is desired.

Finally, Applicants respectfully traverse the Examiner's objection to the drawings under 37 C.F.R. §1.83(a). Figures 1, 2a, 2b and 9 clearly show all features of the invention. In particular, Figure 1 shows the instruction decoder 2, the instruction execution unit 3, 4, and control signals 11, 12. Additionally, Figure 9 shows the various periods while Figures 2a and 2b show the instructions. Additionally, Figure 9 shows a fourth period (t7) starting after a lapse of time from a third period (t4) (see line I01)BRA (at time t7 indicated as E/M). Additionally, Figure 1 shows registers 30-33. Also Figures 2a, 2b show the various fields 401, 404, 402, 405, 403 and 406 as claimed in claim 21. It is therefore respectfully submitted that the drawings show every feature of the invention specified in the claims. It is therefore respectfully requested that the Board reverses the objection to the drawings.

For all of the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case since it is respectfully submitted that the Examiner's rejection of claims 1-25 and objection to the drawings are in error.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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Date: March 14, 2003

TechEncyclopedia

More than 20,000 IT terms

Results found for: operation code

operation code

The part of a machine instruction that tells the computer what to do, such as input, add or branch. The operation code is the verb; the operands are the nouns.

Search TechWeb For:
- operation code

■ TERMS SIMILAR TO YOUR ENTRY

Entries before operation code
- Open With
- Opera
- operand
- operating system
- operational data store

Entries after operation code
- operations
- operations manager
- operations research
- operator
- operator overloading

■ DEFINE ANOTHER IT TERM

Define

Or get a random definition

TechEncyclopedia

More than 20,000 IT terms

Results found for: instruction

instruction

(1) A statement in a programming language.

(2) A machine instruction.

■ TERMS SIMILAR TO YOUR ENTRY

Entries before instruction

- instant messaging
- instant messenger
- instant print
- instant replay
- Institute for Certification

Entries after instruction

- instruction cycle
- instruction mix
- instruction register
- instruction repertoire
- instruction set

■ DEFINE ANOTHER IT TERM

Define

Or get a random definition

TechEncyclopedia

More than 20,000 IT terms

Results found for: machine instruction

machine instruction

An instruction in machine language. Its anatomy is a verb followed by one or more nouns:

OPCODE OPERANDS (one or more)

The op code is the operation to be performed (add, copy, etc.), while the operands are the data to be acted upon (add-a-to-b). There are always machine instructions to INPUT and OUTPUT, to process data by CALCULATING, COMPARING and COPYING it, and to go to some other part of the program with a GOTO instruction. See hardware platforms and computer.

Search TechWeb For:
- machine
- instruction

■ TERMS SIMILAR TO YOUR ENTRY

Entries before machine instruction

- machine code
- machine cycle
- machine dependent
- machine independence
- machine independent

Entries after machine instruction

- machine language
- machine readable
- Macintosh
- Macintosh clone
- Macintosh extension

■ DEFINE ANOTHER IT TERM

Define

Or get a random definition